Digital Design Diploma

# **Assignment 3**

# **Sequential Logic Design**

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| **Group** | G2 |

**Submitted to: Eng. Kareem Waseem**

1. **DFF with clock enable and PRE control signal:**

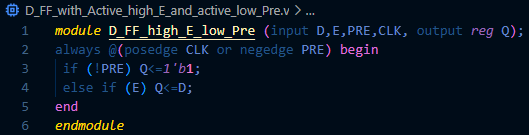
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Figure1: Q1 Code

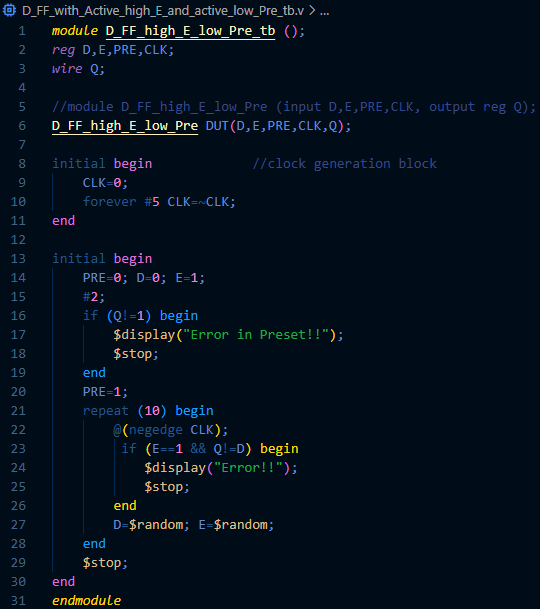
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Figure 2: Q1 Testbench

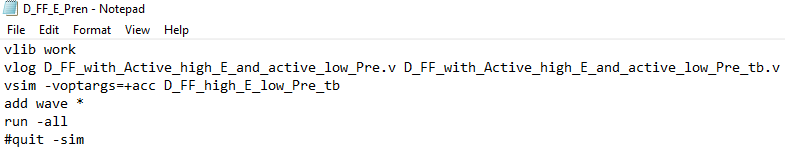
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Figure 3: Q1 DO File

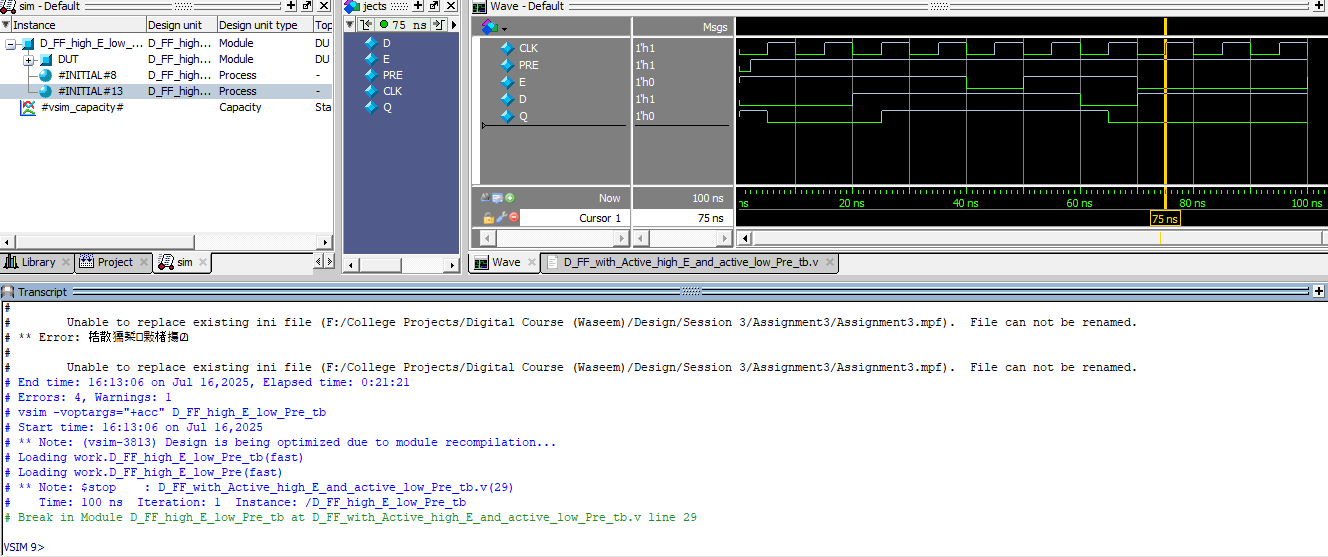
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Figure 4: Q1 Wave

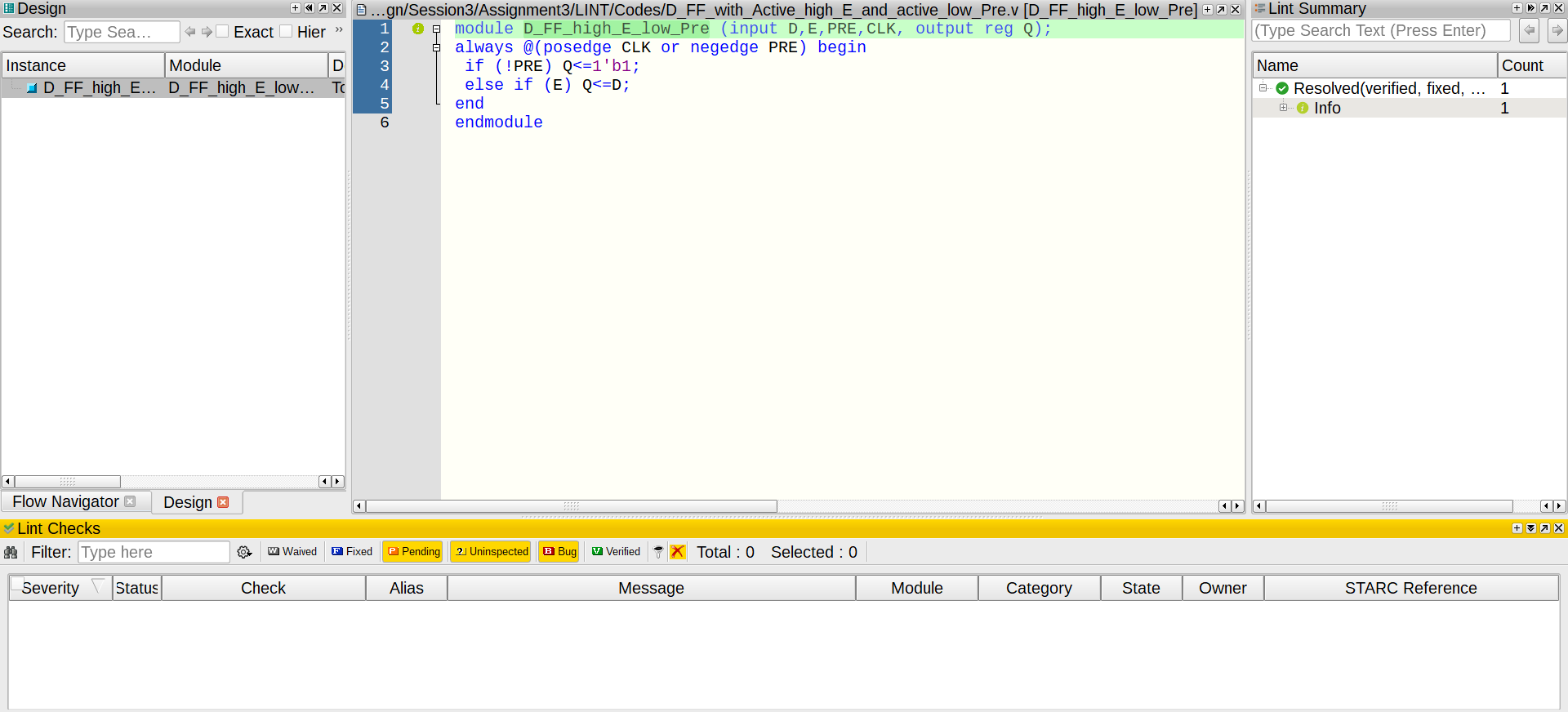
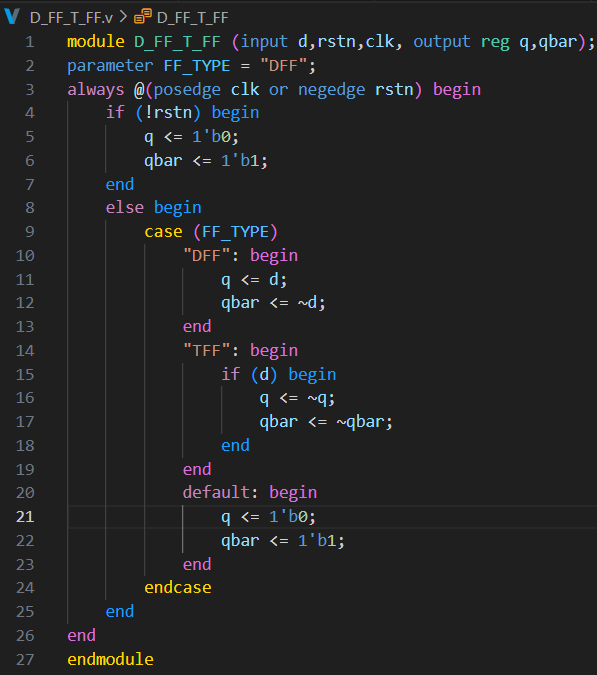
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Figure 5: Q1 Linting

1. **Parameterized Asynchronous FF with Active low rst (D FF & T FF):**

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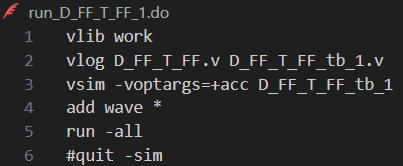
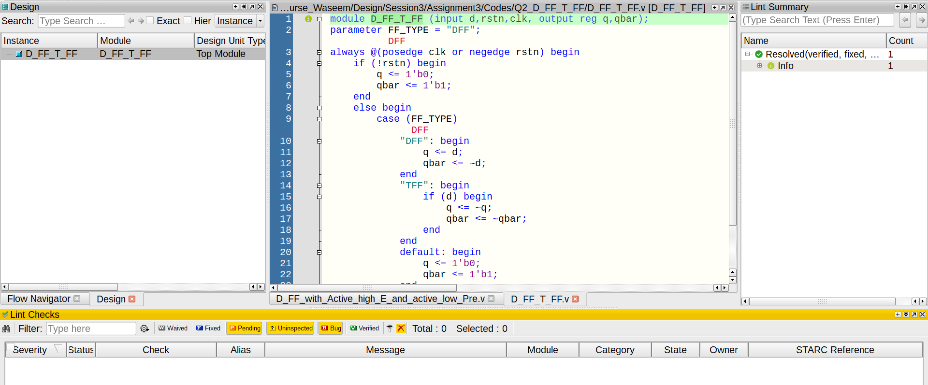
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Figure 6: Q2 Code

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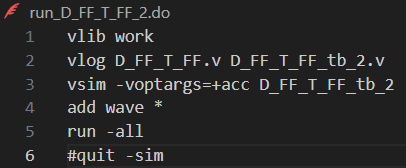
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Figure 9: Q2 Linting

Figure 7: Q2 DO File (DFF)

Figure 8: Q2 DO File (TFF)

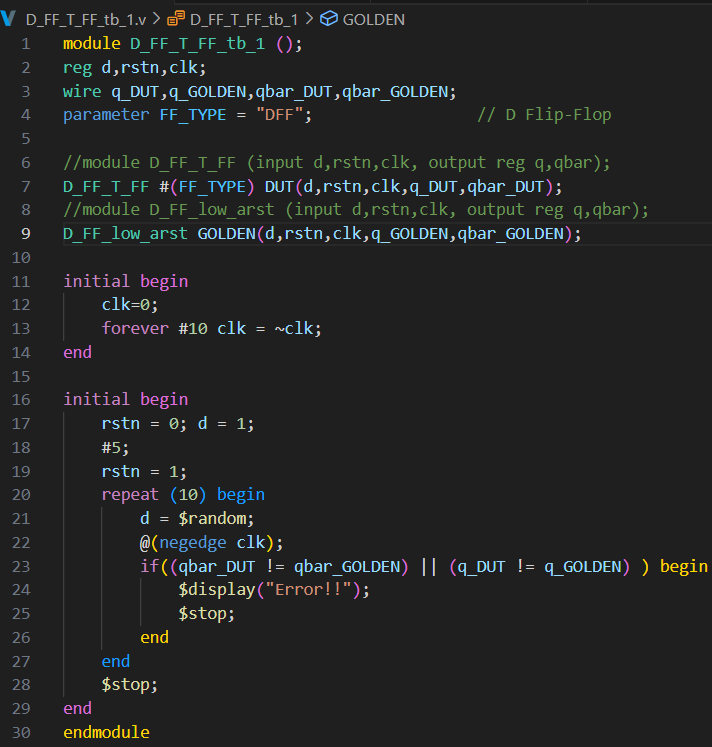
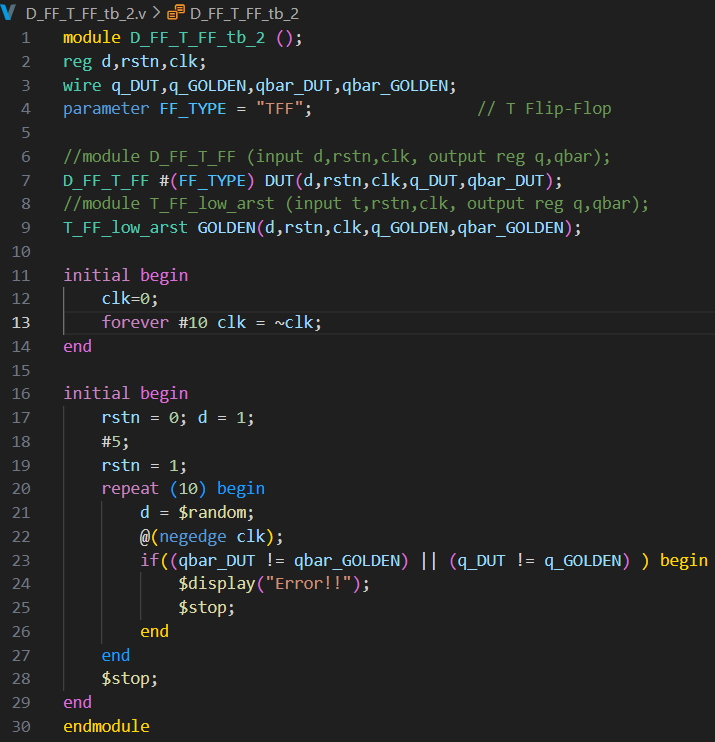
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Figure 11: Q2 Testbench (TFF)

Figure 10: Q2 Testbench (DFF)

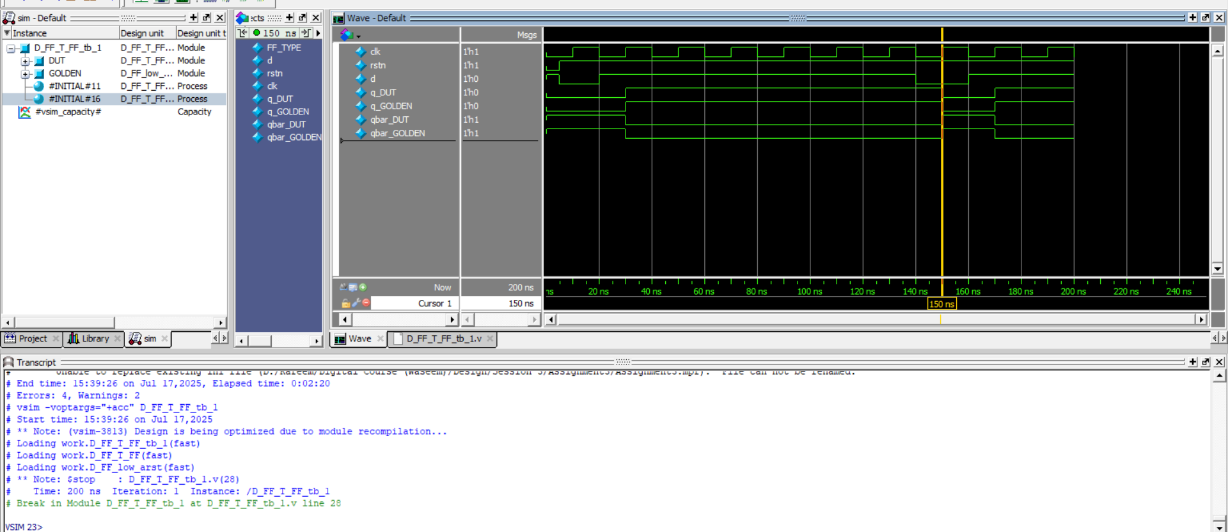
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Figure 12: Q2 Wave (DFF)

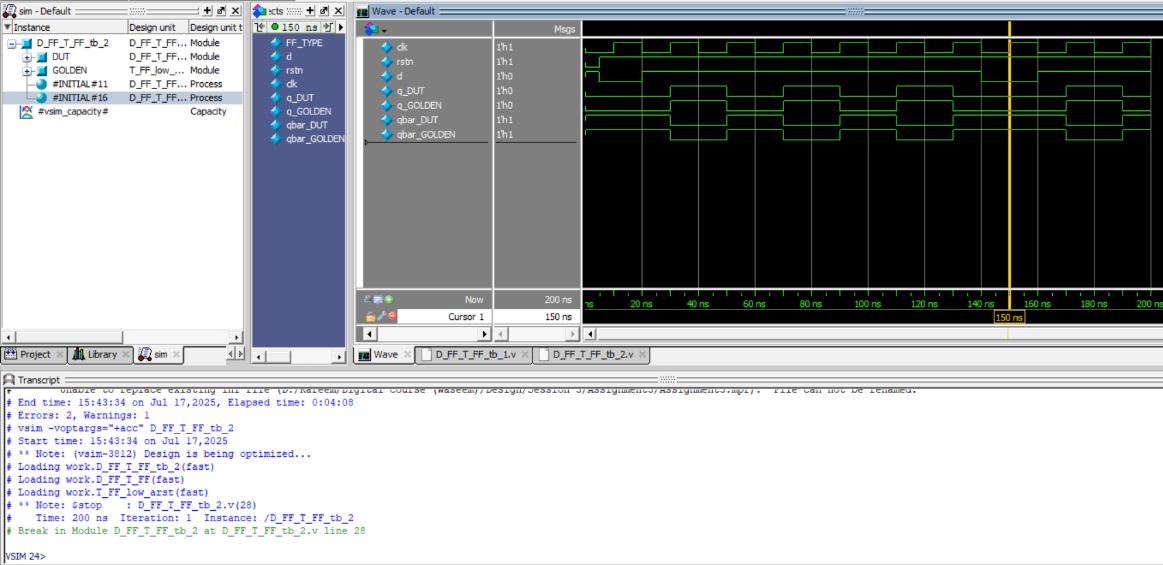
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Figure 13: Q2 Wave (TFF)

1. **BCD up counter (MOD 10 counter):**

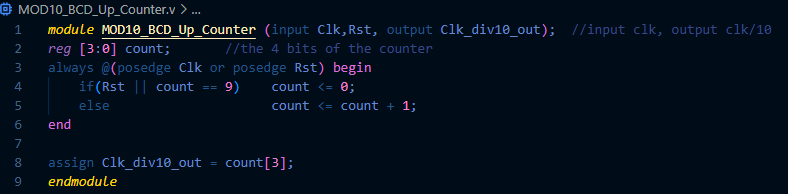
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Figure 14: Q3 Code

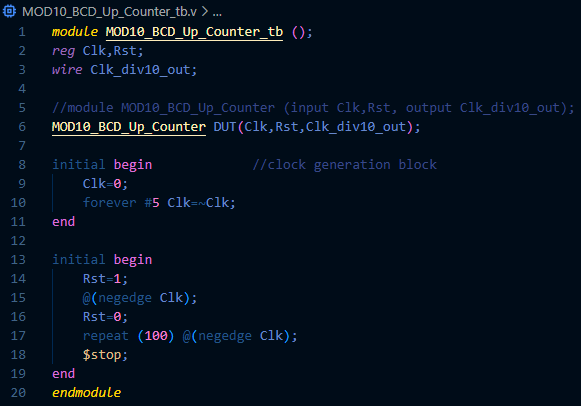
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Figure 15: Q3 Testbench

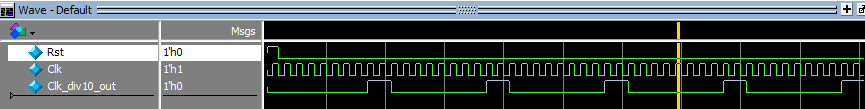
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Figure 16: Q3 Wave

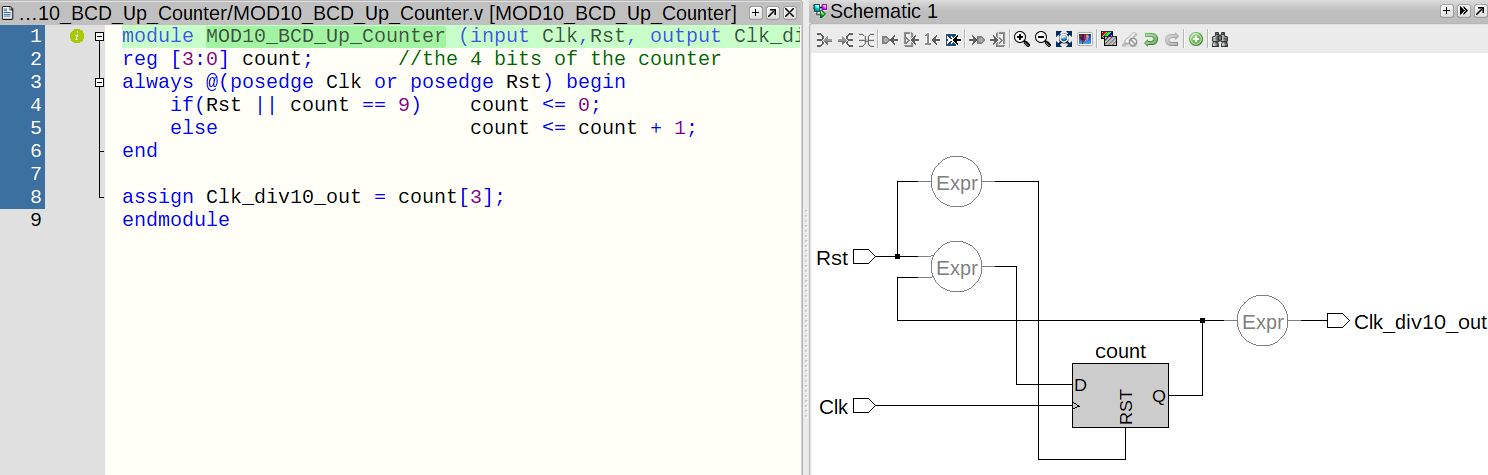
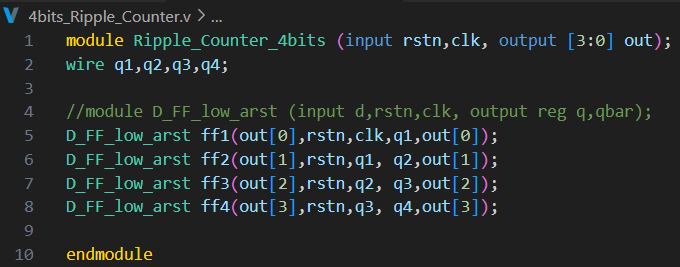
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Figure 17: Q3 Linting

1. **4-bit Ripple Counter:**

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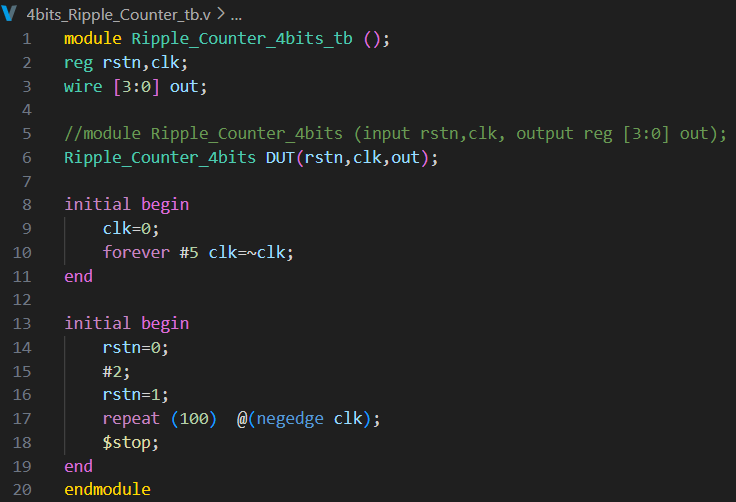
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Figure 18: Q4 Code

Figure 19: Q4 Testbench

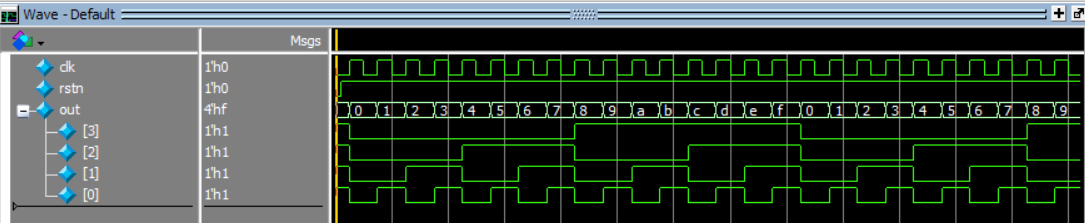
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Figure 20: Q4 Wave

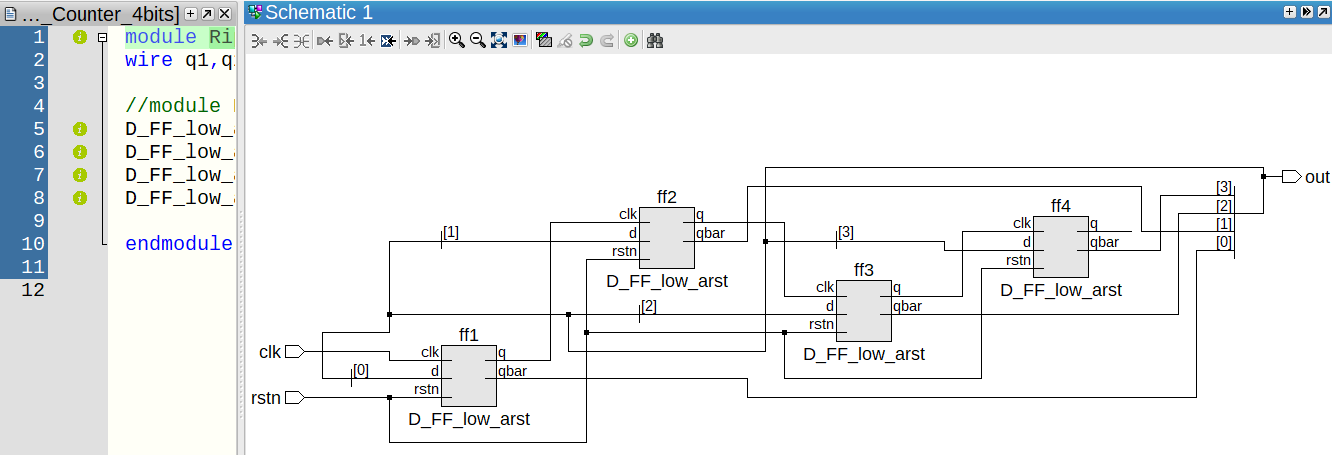
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Figure 21: Q4 Linting

1. **Parameterized Shift register:**

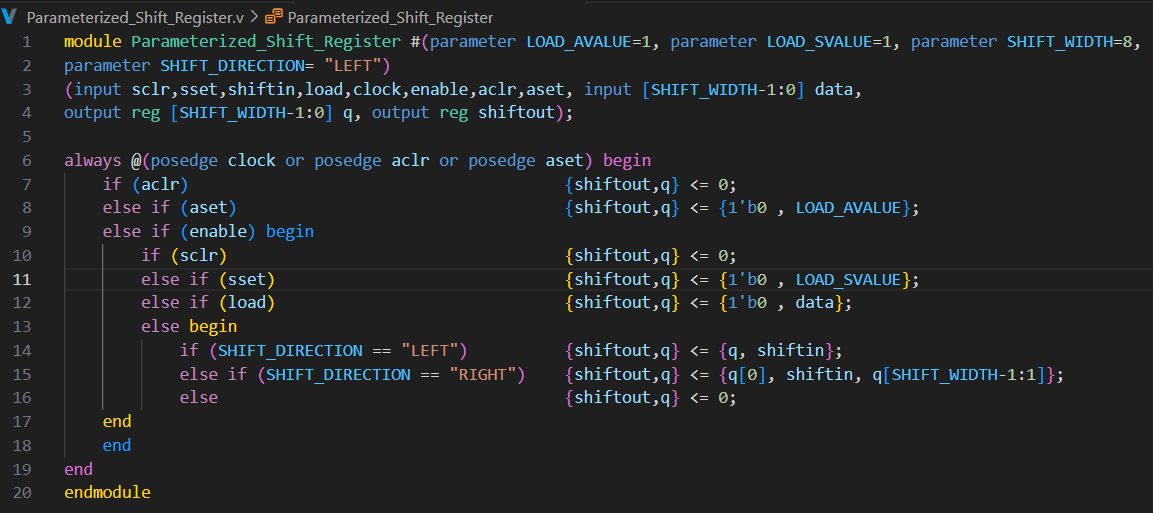
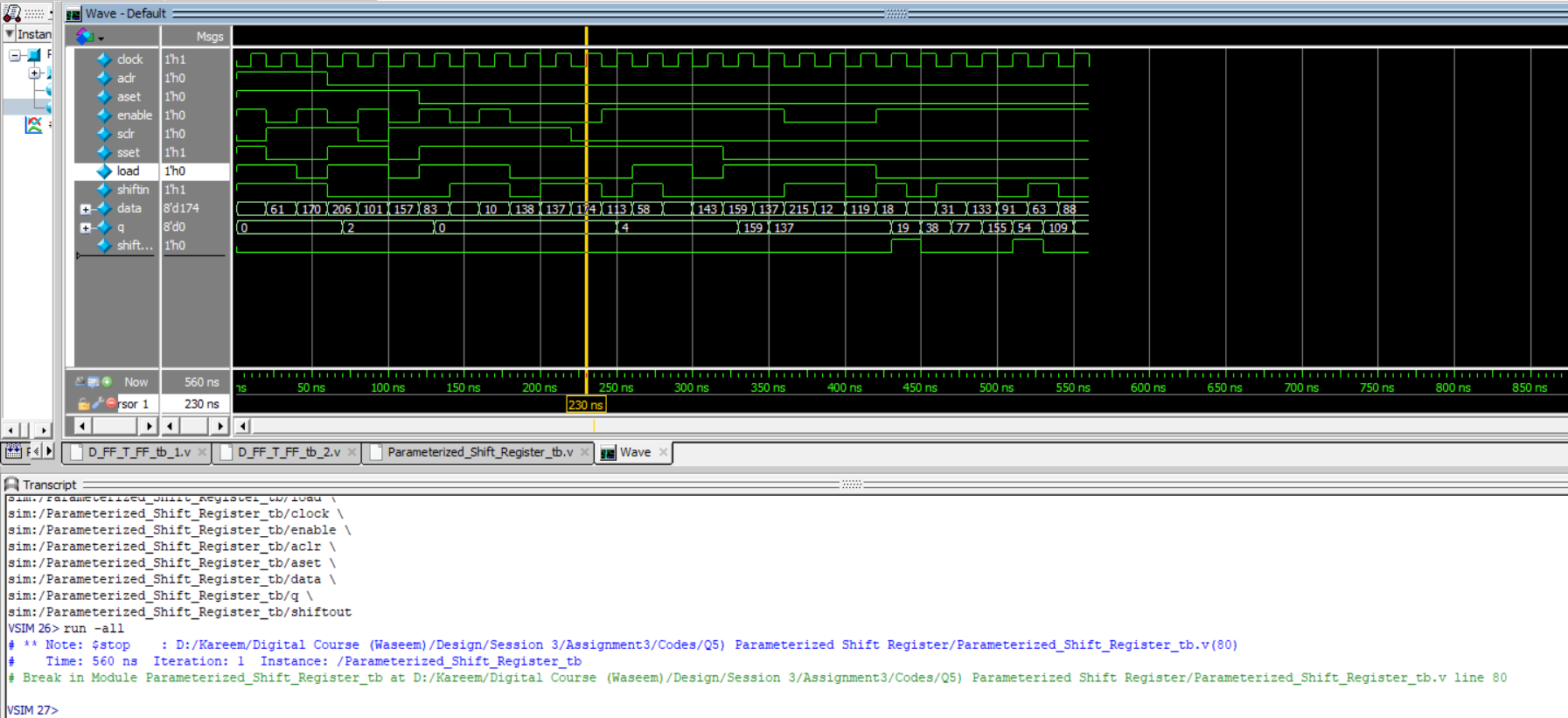
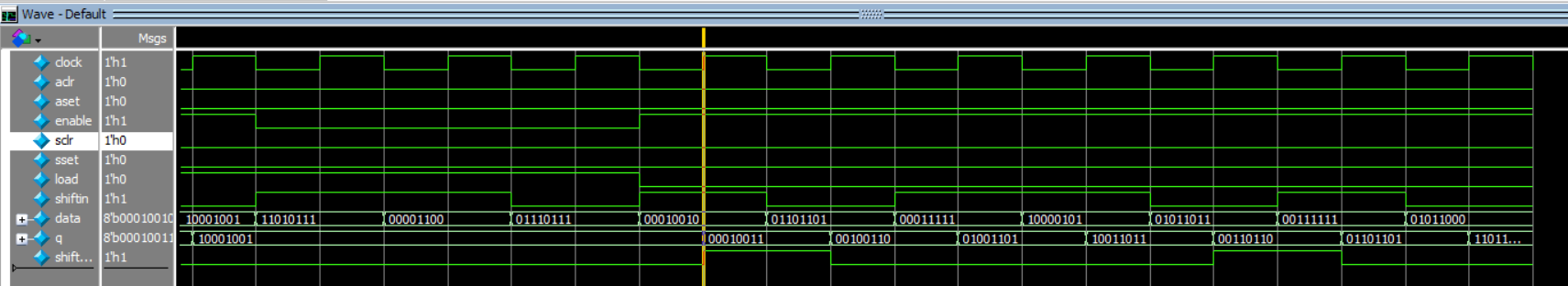
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Figure 24: Q5 Wave (Shifting Part)

Figure 23: Q5 Wave

Figure 22: Q5 Code

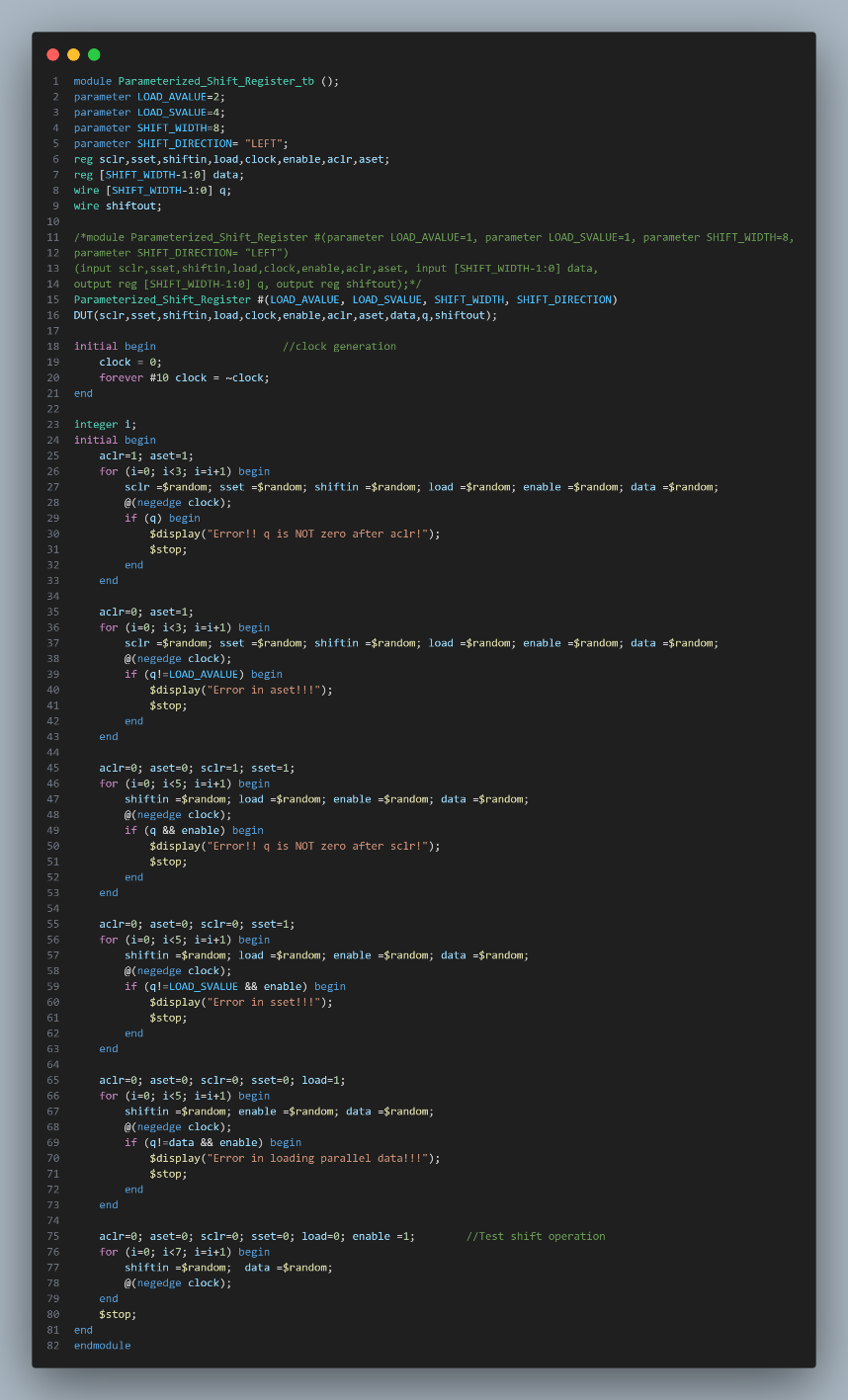
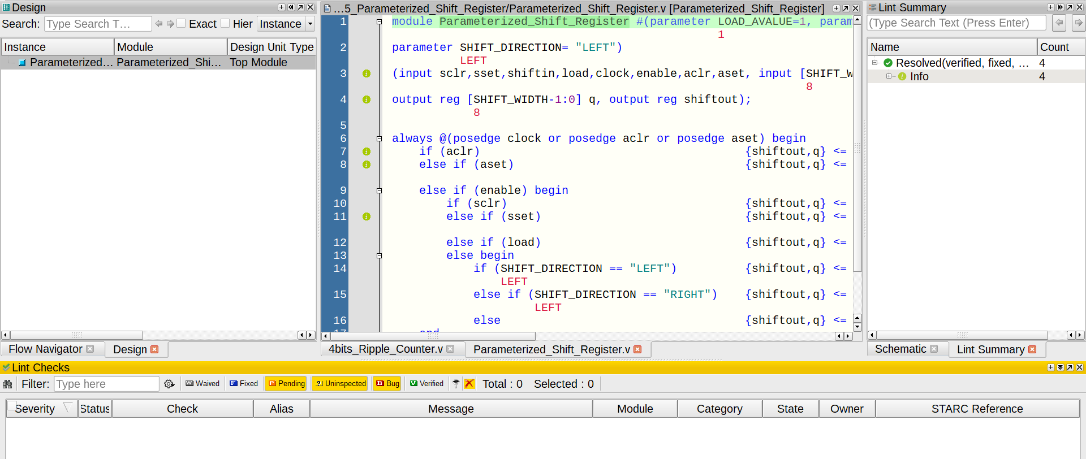
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Figure 26: Q5 Linting

Figure 25: Q5 Testbench

1. **SLE (Sequential Logic Element):**

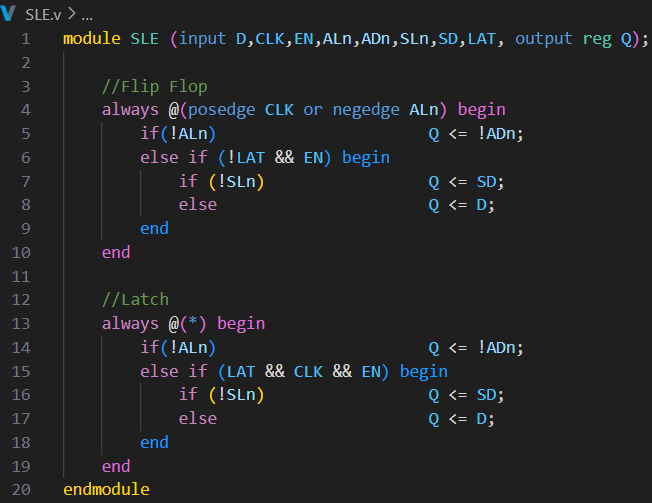
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Figure 27: Q6 Code

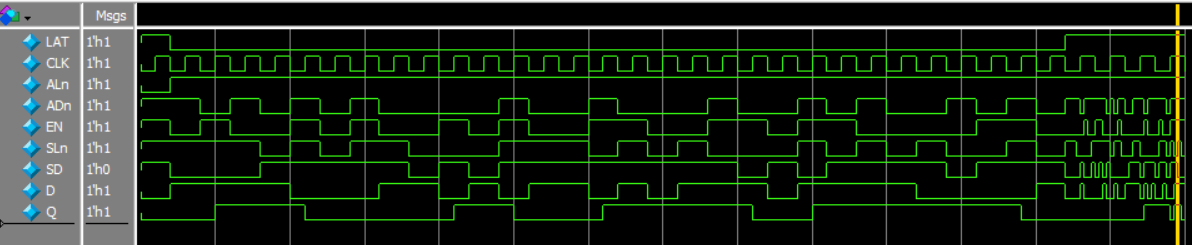
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Figure 28: Q6 Wave

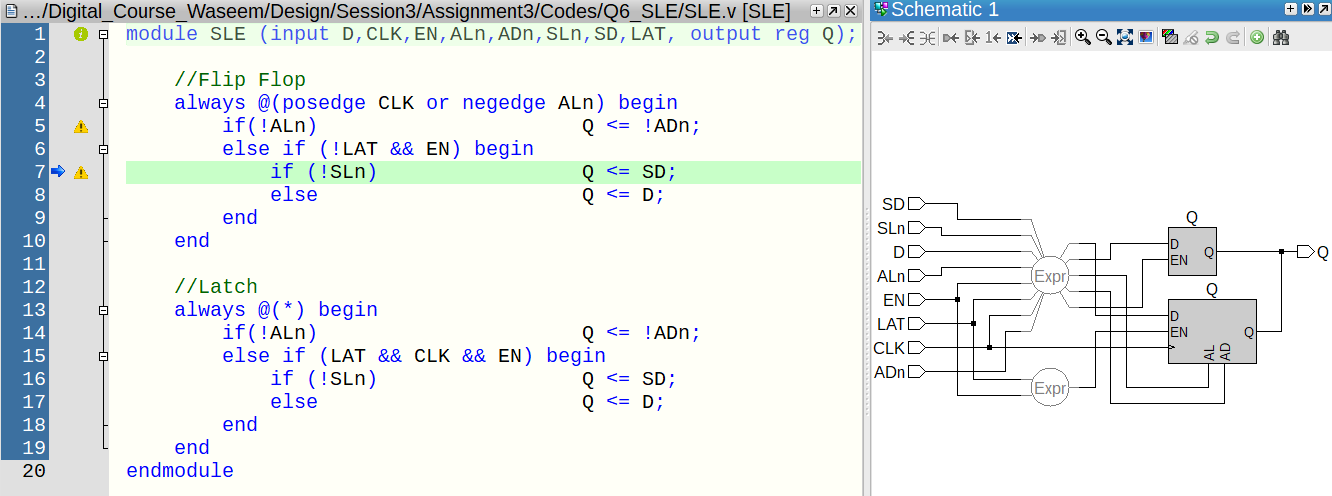
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Figure 29: Q6 Linting

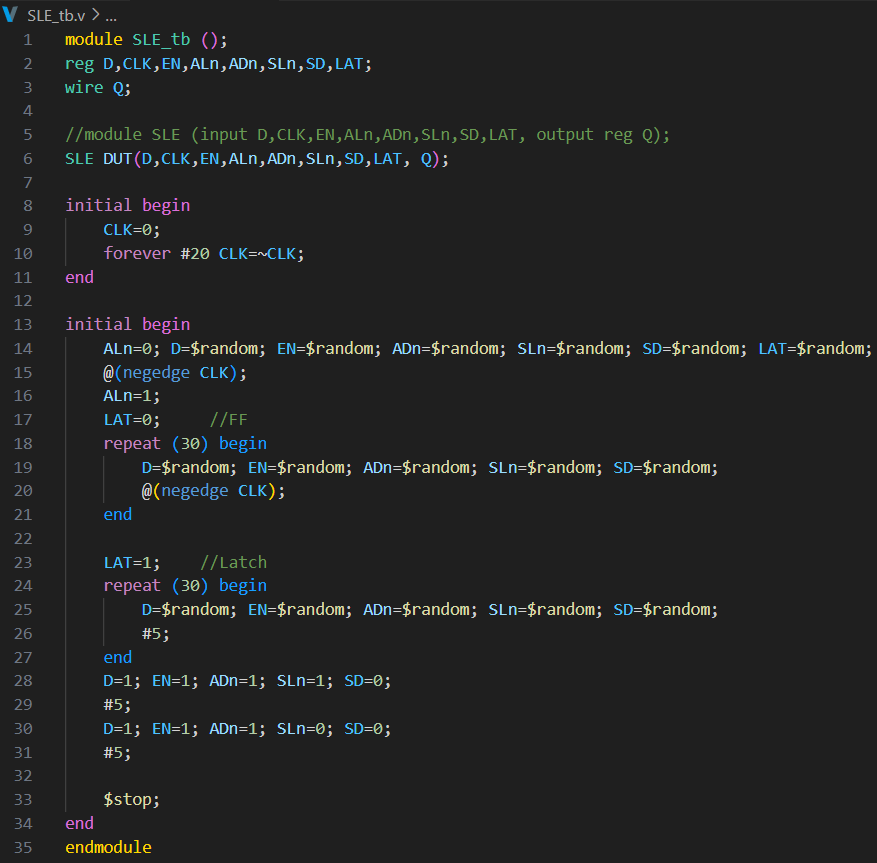
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Figure 30: Q6 Testbench